KLauS6 ASIC Tests for Potential Use in Long Baseline Neutrino Experiments

David Setiawan COL'23, Professor Christopher Mauger
Penn Undergraduate Research Mentoring Program, Department of Physics and Astronomy

INTRODUCTION

As the specifications of the Deep Underground Neutrino Experiment (DUNE) continue to be discussed, Heidelberg University's KLauS6 ASIC is being considered for the readout chip of the 3D-Projection Scintillator Tracker (3DST) of DUNE's near detector. This summer, I tested several components of the KLauS6 chip to verify that the chip behaves properly and is in working order.

ROLE OF KLAUS6 IN DUNE

Neutrino Oscillations
Neutrinos are very small, light, neutral, and abundant elementary particles. They tend not to interact with matter, making them difficult to study. There are 3 types of neutrinos that have been observed: the electron, muon, and tau. An interesting phenomena observed in them is neutrino oscillation where a neutrino changes its type, through weak interactions, as it traverses space.

DUNE
DUNE will study neutrino oscillations by sending a beam of neutrinos from Fermilab to Sanford Underground Research Facility (1300 km apart) and utilizing a near and far detector to collect data. The near detector will be located near the beam source at Fermilab and will measure the initial flux of one type of neutrinos. The far detector will be located at Sanford where it will measure the fluxes of the resulting types of neutrinos.

3DST in DUNE
3DST is a component of the near detector which contains a 3D array of scintillator cubes. When a charged particle interacts with the cubes, photons are emitted and are directed to Silicon Photomultipliers (SiPM), which convert the photons to electrical signals. The signals are then sent to readout chips, which process and forward event information to a computer for analysis. KLauS6 is being considered for the role of this readout chip.

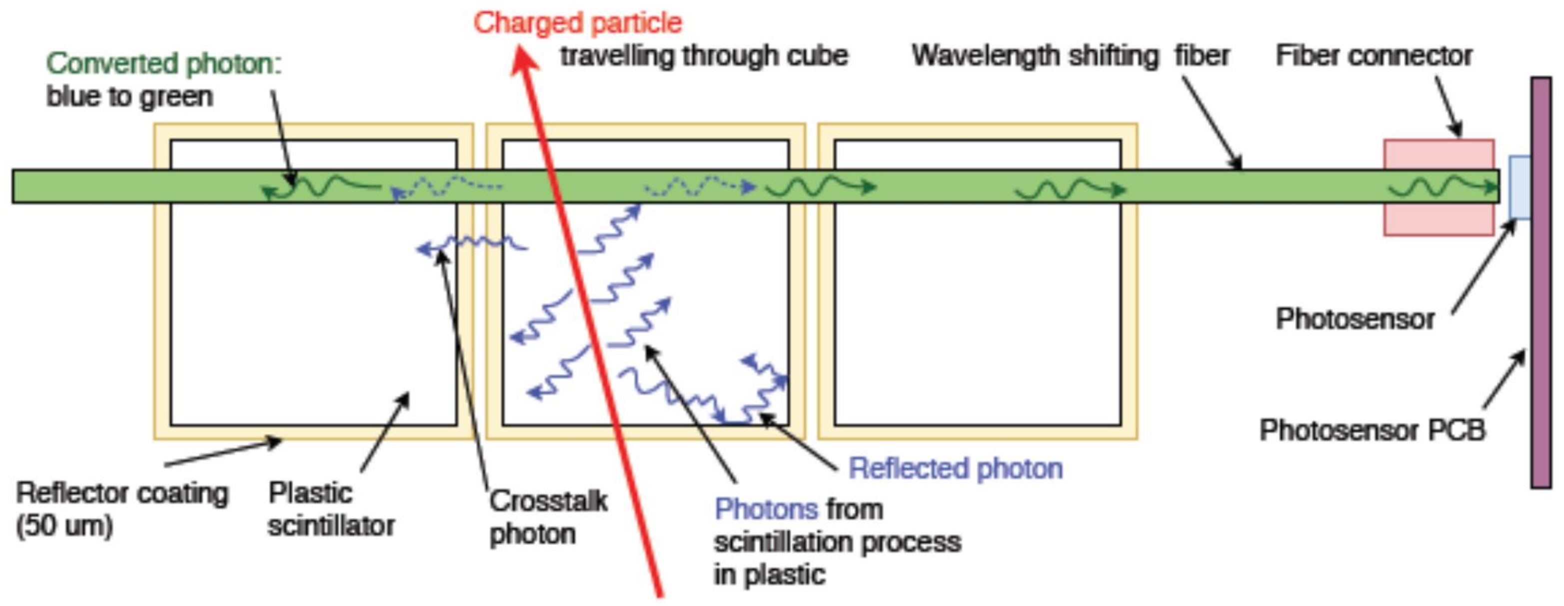

Figure 1. The process of detecting a charged particle passing through the scintillating cubes of the 3DST.

RESULTS

- Features tested with noise hits
  - ADC plots show hits at around 700 bins (expected)
  - Record noise hits only on external trigger pulse
  - Channel threshold calibration
  - Observe some expected timing behavior with noise
- Features tested with SiPM test pulse
  - ADC plots show hits above 700 bins
  - Observed some expected timing behavior (still being investigated)

OBSERVED TIMING BEHAVIOR WITH NOISE HITS

- ASIC configuration used: external trigger disabled, all channels masked except channel 0, threshold set below noise level
- Figure 2. shows the synchronous nature of the channel's busy state with the system clock of 40MHz (25 ns period).
- The peak shown in Figure 3. is measured to be 2304 bins, which is about 450 ns. This is consistent with the busy state duration estimation of around 500 ns and with the synchronization with the system clock as a multiple of 25 ns.

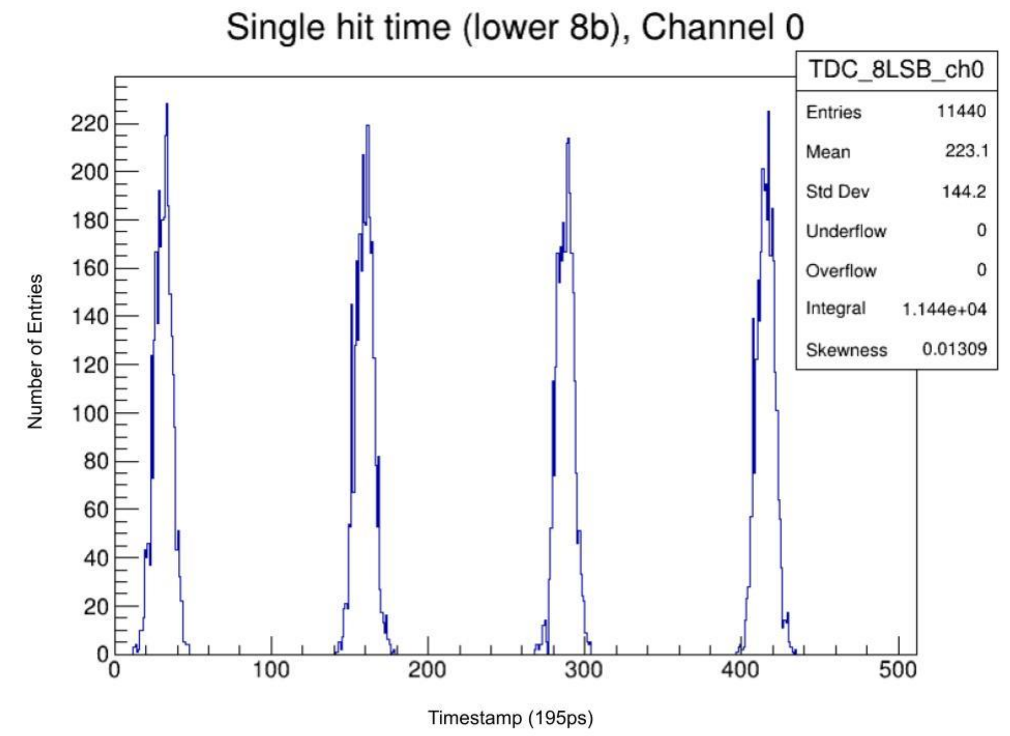

Figure 2. Single hit time plot for channel 0 showing the lower 9-bit timestamp values, in 195 ps bins, and the number of noise hits for each bin.

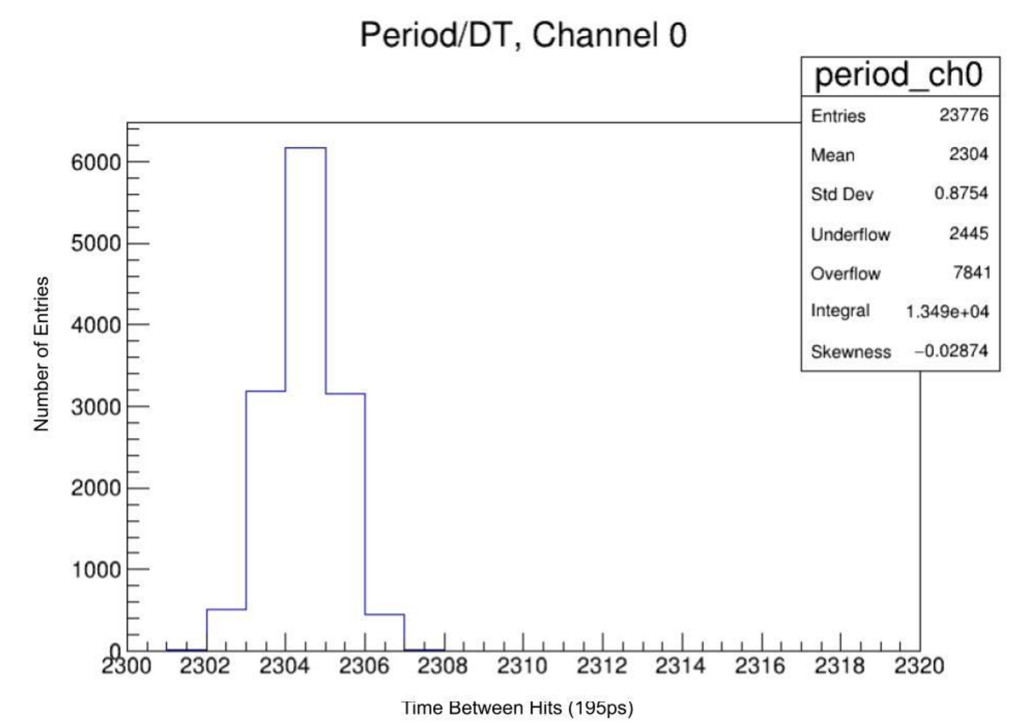

Figure 3. Period plot for channel 0 showing the time between two consecutive hits, in 195 ps bins, and the number of noise hits for each bin.

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OBSERVED TIMING BEHAVIOR WITH SIPM TEST PULSE

- ASIC configuration used: external trigger disabled, all channels unmasked with thresholds set above noise level, SiPM input DAC = 127 (nominal), global threshold = 20
- Test pulse specifications used: varying period, 1.5V amplitude, 50% duty cycle, 10 ns rise and fall time
- About 5000-6000 entries taken for each test pulse period trial
- When using a test pulse with a set period, we expect the time between two consecutive hits to be that period. This behavior can be seen in Figure 4.
- The results of Figure 5. show the busy state blocking new hits and are consistent with the potential 450 ns long busy state found in Figure 3.

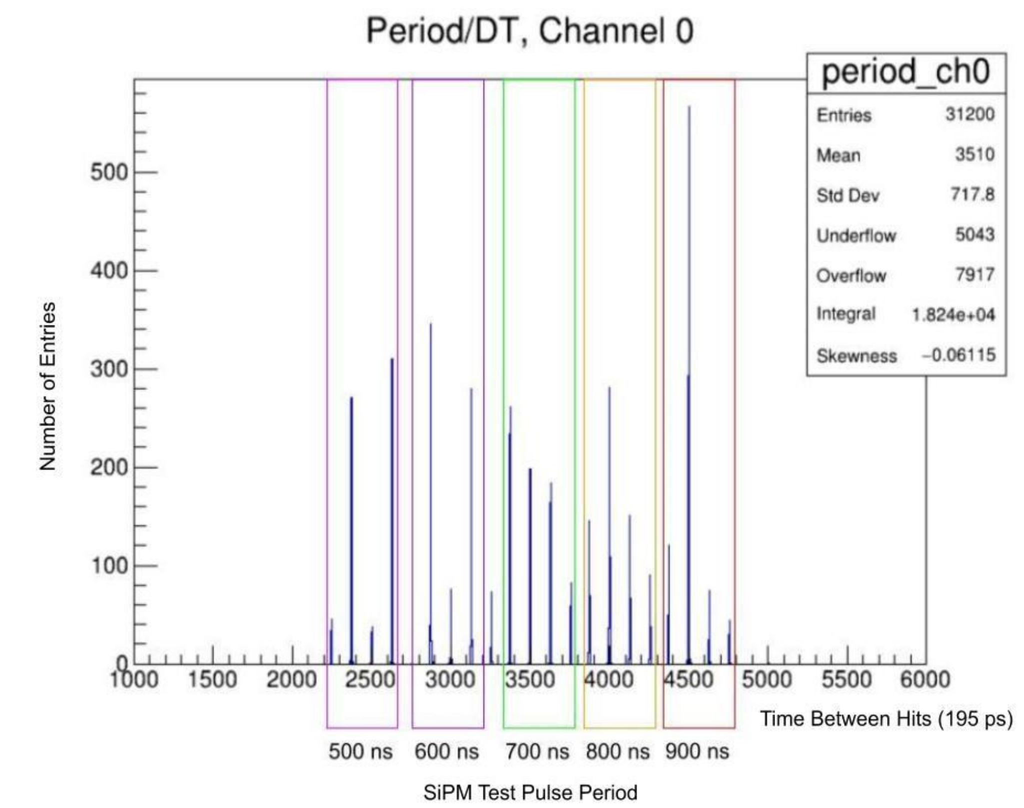

Figure 4. Period plot for channel 0 showing the time between two consecutive hits, in 195 ps bins, and the number of SiPM test pulse hits for each bin. The peaks enclosed by the colored rectangles indicate the resulting peaks when configuring the test pulse to the corresponding period. Test pulse periods range from 500 ns to 900 ns, in 100 ns increments

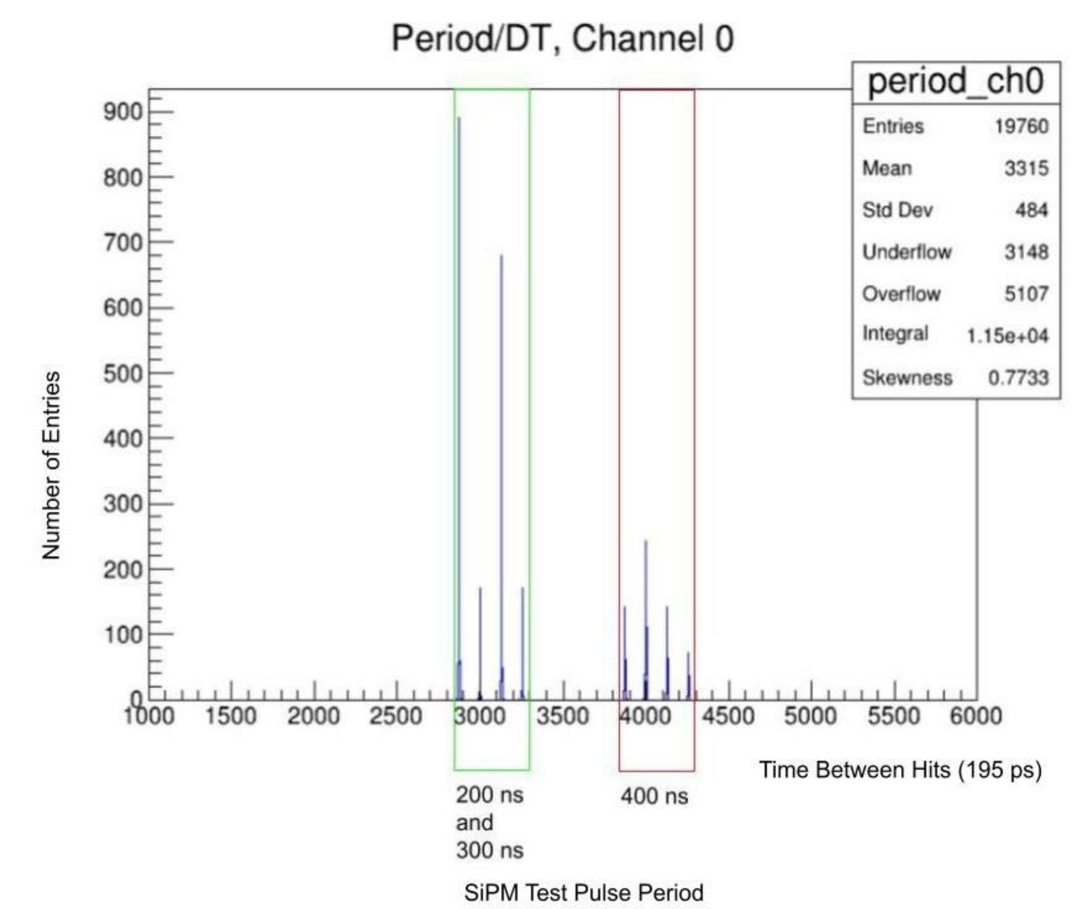

Figure 5. Period plot for channel 0 showing the time between two consecutive hits, in 195 ps bins, and the number of SiPM test pulse hits for each bin. The peaks enclosed by the colored rectangles indicate the resulting peaks when configuring the test pulse to the corresponding period. Test pulse periods range from 200 ns to 300 ns, in 100 ns increments

ACKNOWLEDGMENTS

I would like to thank Professor Mauger for his invaluable mentorship throughout my research this summer. I would also like to thank the Mauger research group and the High Energy Physics Experimental Group for their support and for sharing their expertise.